IN THE DRAWINGS

The attached sheets of drawings includes changes to Figs. 1, 5, 9, and 10. These sheets, which include Figs. 1, 5, 9, and 10, replace the original sheets including Figs. 1, 5, 9, and 10.

Attachment: Replacement Sheets

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1 and 5-20 are pending in this application, Claims 2-4 having been canceled without prejudice or disclaimer, and Claims 1, 9, 13, 16, and 18 having been presently amended. Support for amended Claims 1, 9, 13, 16, and 18 can be found, for example, in the original claims, drawings, and specification as originally filed.[1] Applicants respectfully submit that no new matter has been added.

In the outstanding Office Action, the drawings were objected to due to informalities; Claims 9-20 were rejected under 35 U.S.C. §112, second paragraph; Claims 1-15 were rejected under 35 U.S.C. §101; and Claims 1-20 were rejected under 35 U.S.C. §103(a) as unpatentable over JP 03-204721, JP 2000-276330, and Patel et al. (U.S. Patent No. 6,285,761, herein "Patel").

In response to the objection to the drawings, Applicants have amended Figures 1, 5, 9, and 10 to correct the informality noted in the outstanding Office Action. Accordingly, Applicants respectfully submit that the objection to the drawings has been overcome.

In response to the rejection of Claims 9-20 under 35 U.S.C. §112, second paragraph, Applicants have amended these claims to correct the informality noted in the outstanding Office Action. Accordingly, Applicants respectfully submit that the rejection of Claims 9-20 under 35 U.S.C. §112, second paragraph, has been overcome.

In response to the rejection of Claims 1-15 under 35 U.S.C. §101, Applicants respectfully submit that the rejection of Claims 1-15 is improper as these claims clearly recite apparatus claim limitations and define articles of manufacture. Further, Claims 1-15 recite devices providing a concrete, useful, and tangible result. Amended Claim 1 does not merely

[1] See page 10, lines 13-25 of the specification; original Claims 2 and 3; and Figure 2.

recite a mathematical algorithm without a practical application, but is rather directed to an article of manufacture for generating random numbers which can be used, for example, in cryptographic devices as described in Applicants' specification.

Furthermore, the Examiner's attention is invited to the *State Street Bank* decision, in which the Court of Appeals for the Federal Circuit held that the transformation of monetary data from one form into another constitutes a practical application of a mathematical algorithm to produce a useful, concrete, and tangible result. Thus, an article of manufacture for generating random numbers is also statutory.

MPEP § 2106 further provides that:

> Office personnel have the burden to establish a *prima facie* case that the claimed invention as a whole is directed to solely an abstract idea or to manipulation of abstract ideas or does not produce a useful result. Only when the claim is devoid of any limitations to a practical application in a technological arts should it be rejected under 35 U.S.C. § 101 . . . Further, when such a rejection is made, office personnel must expressly state how the language of the claims has been interpreted to support the rejection. (Emphasis added.) See MPEP § 2106.

Accordingly, Applicants respectfully request that the rejection of rejection of Claims 1-15 under 35 U.S.C. §101 be withdrawn.

In response to the rejection of Claims 1-20 under 35 U.S.C. §103(a) as unpatentable over JP 03-204721, JP 2000-276330, and Patel, Applicants have amended independent Claim 1 to include features of Claims 2 and 3 and additional distinguishing features. Applicants respectfully submit that amended independent Claim 1 recites novel features clearly not taught nor rendered obvious by the applied references.

Amended independent Claim 1 is directed to a seed generating circuit including, *inter alia*:

> ...the oscillating circuit has a first exclusive OR computing circuit, a first inverter circuit, a second exclusive OR computing circuit, and a second inverter circuit, coupled in series in this order,

> data are given to one of input ends of the first exclusive OR computing circuit and to one of input ends of the second exclusive OR computing circuit, respectively, and
>
> the oscillating circuit oscillates when the data inputted to the first and second exclusive OR computing circuits have a specific combination.

The cited references fail to teach or suggest that "the oscillating circuit has a first exclusive OR computing circuit, a first inverter circuit, a second exclusive OR computing circuit, and a second inverter circuit, coupled in series in this order," as recited in Applicants' amended independent Claim 1.

Page 4 of the outstanding Office Action asserts that JP 03-204721 describes "a circuit for generating a random number having an 'oscillating circuit' feature." However, Figures 1-3 of JP 03-204721 only show a self-running counter 103, 303 including one NAND circuit and two invertors connected in series. JP 03-204721 does not describe a series connection of a first exclusive OR computing circuit, a first inverter circuit, a second exclusive OR computing circuit, and a second inverter circuit, arranged in this order respectively.

Further, the self-running counter of JP 03-204721 may oscillate continuously or intermittently; however, the intermittent oscillation is performed by a switch to an oscillating circuit. The randomness of the output of the self-running counter 103, 303 depends on the unstableness of an oscillation pulse after the start of oscillation. In addition, Applicants submit that in recent LSI technologies, the signal instability of logic circuits is quite small, and therefore, sufficient randomness of numbers cannot be obtained by only utilizing the signal instability of logic circuits.

In contrast, one advantageous feature of Applicants' invention is that the randomness of the output of the oscillating circuit depends not only on the unstableness of the oscillation pulse, but also on an initial value Z of the circuit. Page 10, line 26 to page 11, line 10 of Applicants' specification describes that:

> Furthermore, the outputs of the circuit expressed in FIG. 2 change corresponding to the value of the initial value Z, unlike a simple oscillating circuit. That is, in the case where the initial value Z is "1", both of outputs Q1 and Q2 become "0" when the inputs X1 and X2 are "1", and the output Q1 becomes "1" and the output Q2 becomes "0" when the inputs X1 and X2 are "0".
>
> On the other hand, in the case where the initial value Z is "0", both of outputs Q1 and Q2 become "1" when the inputs X1 and X2 are "1", the output Q1 becomes "0" and the output Q2 becomes "1" when the inputs X1 and X2 are "0".

The initial value Z is decided by a final output (random value) of the circuit when the circuit stops the last oscillation, and by a combination of signals X1 and X2 inputted next. Separate random signals can be used for X1 and X2. Therefore, according to an embodiment of Applicants' invention, the initial value Z can always be random. Further, the output randomness of the oscillating circuit can be greatly improved by the multiplying effect of the randomness of the initial value Z and the randomness generated by stopping the oscillating circuit. In order to store the output of the oscillating circuit when the circuit stops, a unique circuit as recited in Applicants' Claim 1 includes two exclusive OR circuits.

Applicants respectfully submit that JP 2000-276330 and Patel fail to cure any of the above-noted deficiencies of JP 03-204721.

Accordingly, Applicants respectfully submit that amended independent Claim 1 (and all claims depending thereon) patentably distinguishes over JP 03-204721, JP 2000-276330, and Patel.

Amended independent Claims 9, 13, 16, and 18 also recite "the oscillating circuit has a first exclusive OR computing circuit, a first inverter circuit, a second exclusive OR computing circuit, and a second inverter circuit, coupled in series in this order, data are given to one of input ends of the first exclusive OR computing circuit and to one of input ends of the second exclusive OR computing circuit, respectively, and the oscillating circuit oscillates when the data inputted to the first and second exclusive OR computing circuits have a

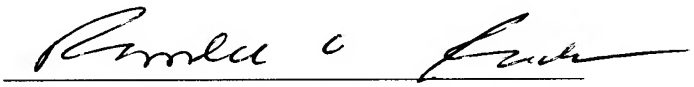
specific combination." Thus, independent Claims 9, 13, 16, and 18 (and all claims depending thereon) are believed to be patentable for at least the reasons discussed above.

Accordingly, Applicants respectfully request the rejection of Claims 1-20 under 35 U.S.C. §103(a) as unpatentable over JP 03-204721, JP 2000-276330, and Patel be withdrawn.

Consequently, in view of the present amendment, and in light of the above discussion, the pending claims as presented herewith are believed to be in condition for formal allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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